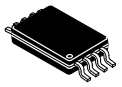
PCS3P73Z01AW

Wide Frequency Range TIMING SAFE™ Peak EMI Reduction IC

ON Semiconductor®

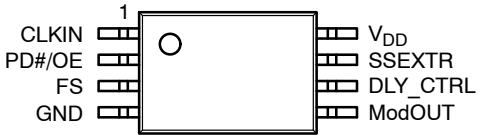
http://onsemi.com



TSSOP−8
T SUFFIX
CASE 948AL

TDFN−8
C SUFFIX
CASE 511AQ

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Description

PCS3P73Z01AW is a 2.5 V / 3.3 V versatile EMI reduction IC based on ON Semiconductor's patent pending Timing−Safe technology. PCS3P73Z01AW accepts one input from an external reference, and locks on to it delivering a 1x Timing−Safe clock. PCS3P73Z01AW has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer to the *Frequency Selection Table* for details. The device has an SSEXTR pin to select different deviation and associated Input−Output Skew (T_{SKEW}), depending upon the value of an external resistor connected between SSEXTR and GND. PCS3P73Z01AW has a DLY_CTRL for adjusting the Input−Output clock delay, depending upon the value of capacitor connected at this pin to GND. PD#/OE provides the Power Down option. Outputs will be tri−stated when power down is active.

PCS3P73Z01AW operates from a 2.5 V / 3.3 V supply and is available in an 8 Pin, TSSOP, and TDFN (2X2) COL Packages, over Commercial and Industrial temperature range.

Application

PCS3P73Z01AW is targeted for use in Displays, Camera modules and SDRAM memory interface systems**.**

Features

- 1x, LVCMOS Timing−Safe Peak EMI Reduction
- Input Frequency:
  - 2 MHz − 16 MHz @ 2.5 V
  - 2 MHz − 20 MHz @ 3.3 V
- Output Frequency (Timing−Safe):
  - 2 MHz − 16 MHz @ 2.5 V
  - 2 MHz − 20 MHz @ 3.3 V
- Analog Deviation Selection
- External Input−Output Delay Control Option
- Power Down Option for Power Save Mode
- Supply Voltage:
  - 2.5 V ± 0.2 V
  - 3.3 V ± 0.3 V
- Commercial and Industrial Temperature Range
- 8 pin, TSSOP, and TDFN(2X2) COL Packages
- The First True Drop−in Solution
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

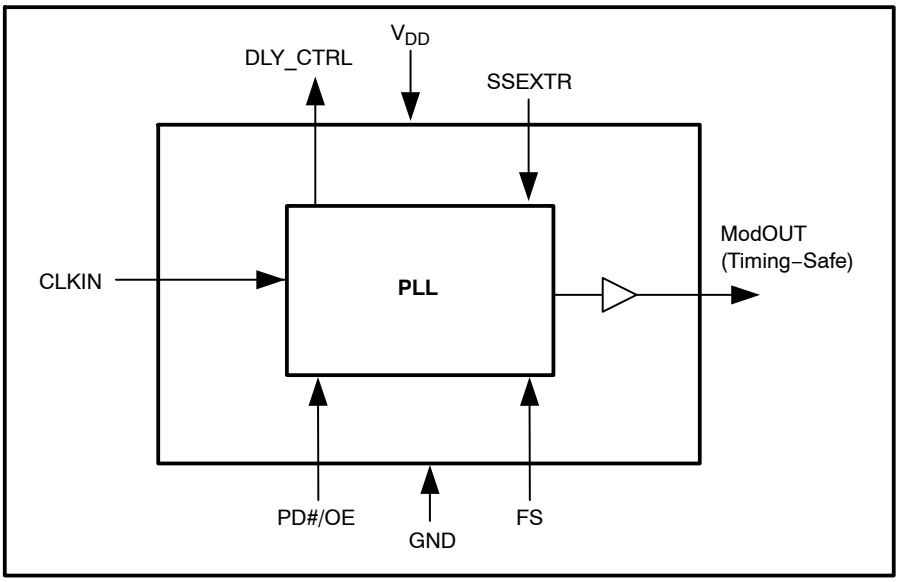


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Type	Pin Name	Description
1	I	CLKIN	External reference Clock input.
2	I	PD#/OE	Power Down. Pull LOW to enable Power Down. Outputs will be tri−stated when power down is enabled. Pull HIGH to disable power down and enable output. There is NO default state.
3	I	FS	Frequency Select. There is NO default state. *See Frequency Selection table for details.*
4	P	GND	Ground
5	O	ModOUT	Buffered modulated Timing−Safe clock output
6	O	DLY_CTRL	External Input−Output Delay control
7	I	SSEXTR	Analog Deviation Selection through external resistor to GND.
8	P	V_{DD}	2.5 V / 3.3 V supply Voltage

Table 2. FREQUENCY SELECTION TABLE

V_{DD}	FS	Frequency (MHz)
2.5 V	0	2−6
	1	6−16
3.3 V	0	2−6
	1	6−20

Table 3. OPERATING CONDITIONS

Parameter	Description		Min	Max	Unit
V_{DD} (3.3 V)	Supply Voltage		2.3	2.7	V
V_{DD} (2.5 V)	Supply Voltage		3	3.6	V
T_A	Operating Temperature	Commercial	0	+70	°C
		Industrial	−40	+85	
C_L	Load Capacitance			10	pF
C_{IN}	Input Capacitance			7	pF

Table 4. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			2.3	2.5	2.7	V
V_{IL}	Input LOW Voltage					0.7	V
V_{IH}	Input HIGH Voltage			1.7			V
I_{IL}	Input LOW Current	V_{IN} = 0 V				50	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	μA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA				0.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA		1.8			V
I_{CC}	Static Supply Current	CLKIN & PD#/OE pins pulled to GND				2	μA
I_{DD}	Dynamic Supply Current (Unloaded Output)	Commercial temp.	FS = 0			6	mA
			FS = 1			7	
		Industrial temp.	FS = 0			8	
			FS = 1			9	
Z_o	Output Impedance				36		Ω

Table 6. SWITCHING CHARACTERISTICS FOR 2.5 V

Parameter	Test Conditions		Min	Typ	Max	Unit
Input Frequency	FS = 0		2		6	MHz
	FS = 1		6		16	
ModOUT	FS = 0		2		6	
	FS = 1		6		16	
Duty Cycle (Notes 1, 2)	Measured at V_{DD} /2		45	50	55	%
Rise Time (Notes 1, 2)	Measured between 20% to 80%			1.7	2.3	nS
Fall Time (Notes 1, 2)	Measured between 80% to 20%			0.9	1.6	nS
Cycle−to−Cycle Jitter (Note 2)	Unloaded output with SSEXTR OPEN	FS = 0; @ 5 MHz		±225		pS
		FS = 1; @ 15 MHz		±150		
Input−to−Output propagation Delay (Note 2)	Unloaded outputs with SSEXTR pin OPEN, No load on DLY_CTRL	FS = 0; @ 6 MHz		175		pS
		FS = 1; @ 12 MHz		75		
PLL Lock Time (Note 2)	Stable power supply, valid clock presented on CLKIN pin				3	mS

1. All parameters are specified with 10 pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$				50	μA
I_{IL}	Input LOW Current	$V_{IN} = 0$ V				50	μA
V_{OH}	Output HIGH Voltage	$I_{OH} = -8$ mA		2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 8$ mA				0.4	V
I_{CC}	Static Supply Current	CLKIN pulled Low, PD#/OE pulled Low				2	μA
I_{DD}	Dynamic Supply Current (Unloaded output)	Commercial temp.	FS = 0			8	mA
			FS = 1			10	
		Industrial temp.	FS = 0			10	
			FS = 1			12	
Z_o	Output Impedance				27		Ω

Table 8. SWITCHING CHARACTERISTICS FOR 3.3 V

Parameter	Test Conditions		Min	Typ	Max	Unit
Input Frequency	FS = 0		2		6	MHz
	FS = 1		6		20	
ModOUT	FS = 0		2		6	
	FS = 1		6		20	
Duty Cycle (Notes 3, 4)	Measured at V_{DD} /2		45	50	55	%
Rise Time (Notes 3, 4)	Measured between 20% to 80%			1.2	1.9	nS
Fall Time (Notes 3, 4)	Measured between 80% to 20%			0.8	1.4	nS
Cycle−to−Cycle Jitter (Note 4)	Unloaded output with SSEXTR OPEN	FS = 0; @ 5 MHz		±200		pS
		FS = 1; @ 15 MHz		±125		
Input−to−Output propagation Delay (Note 4)	Unloaded outputs with SSEXTR pin OPEN, No load on DLY_CTRL	FS = 0; @ 6 MHz		−75		pS
		FS = 1; @ 12 MHz		125		
PLL Lock Time (Note 4)	Stable power supply, valid clock presented on CLKIN pin				3	mS

3. All parameters are specified with 10 pF loaded outputs.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

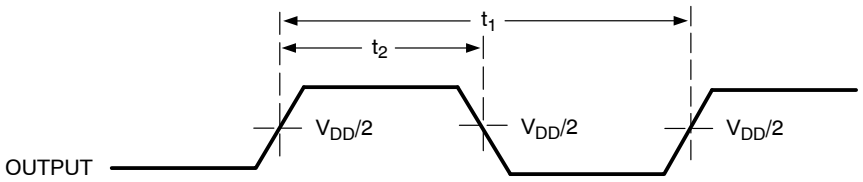


Figure 2. Duty Cycle Timing

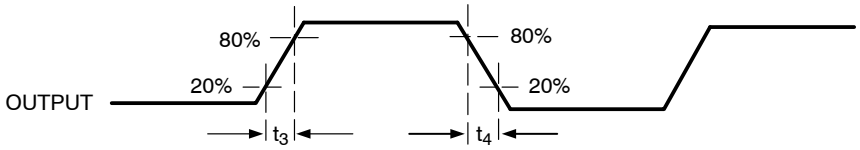


Figure 3. All Outputs Rise/Fall Time

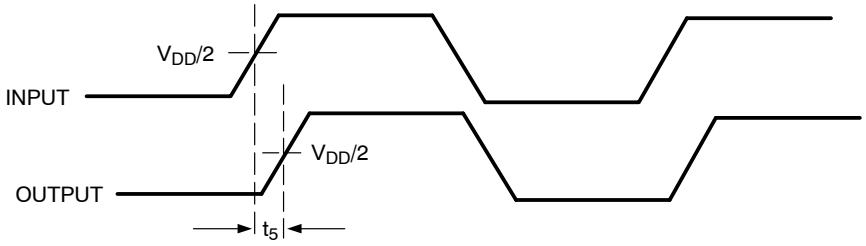
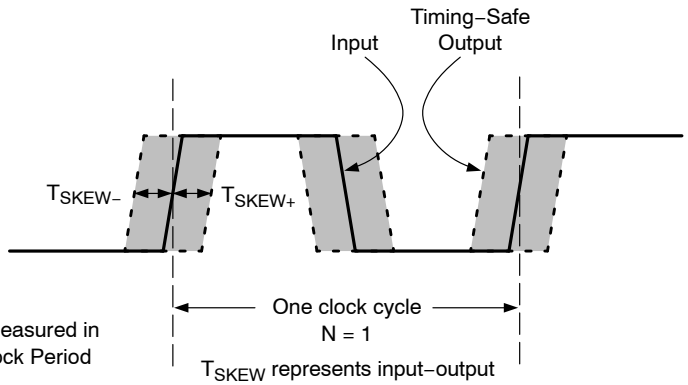


Figure 4. Input − Output Propagation Delay



NOTE: Tskew is measured in units of Clock Period

T_{SKEW} represents input−output skew when Deviation is ON

For example, $T_{SKEW} = \pm 0.20$ for an Input clock of 12 MHz, translates in to (1/12 MHz) * 0.20 = 16.66 nS

Figure 5. Input − Output Skew

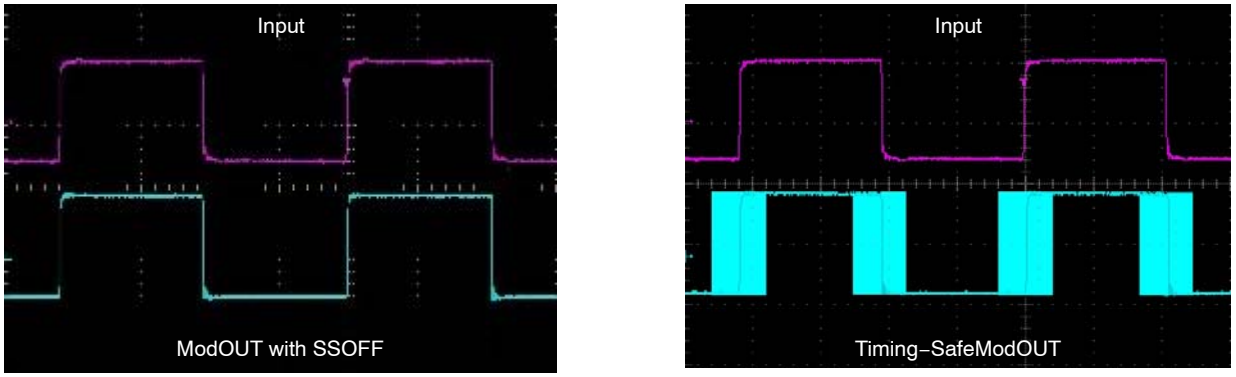


Figure 6. Typical Example of Timing−Safe Waveform

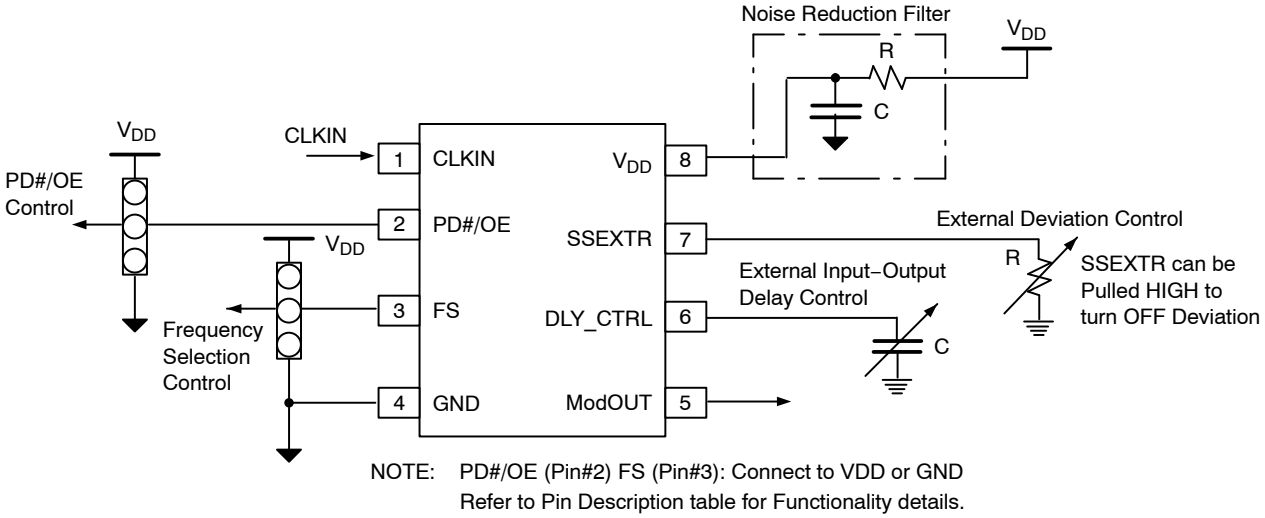


Figure 7. Typical Application Schematic

TYPICAL CHARACTERISTICS (for V_{DD} = 2.5 V ± 0.2 V and 3.3 V ± 0.3 V)

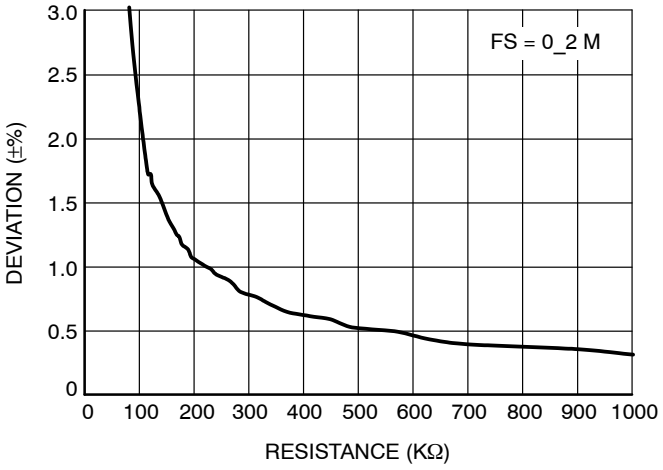


Figure 8. Deviation vs. Resistance (2 MHz, FS = 0)

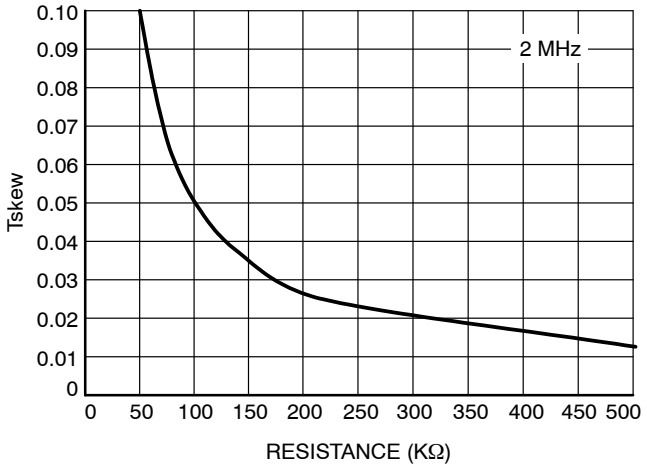


Figure 9. Tskew vs. Resistance (2 MHz, FS = 0)

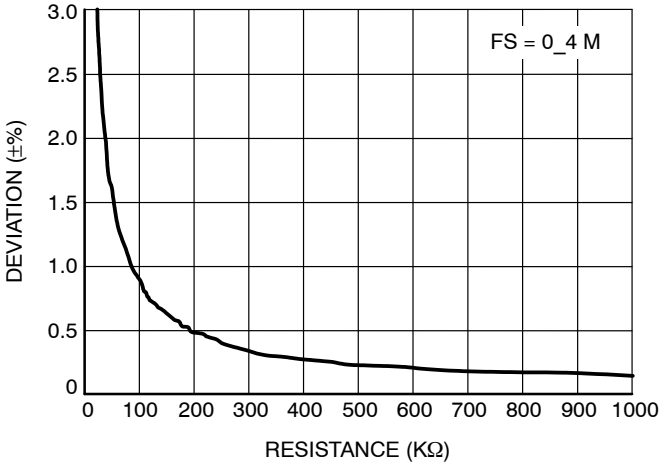


Figure 10. Deviation vs. Resistance (4 MHz, FS = 0)

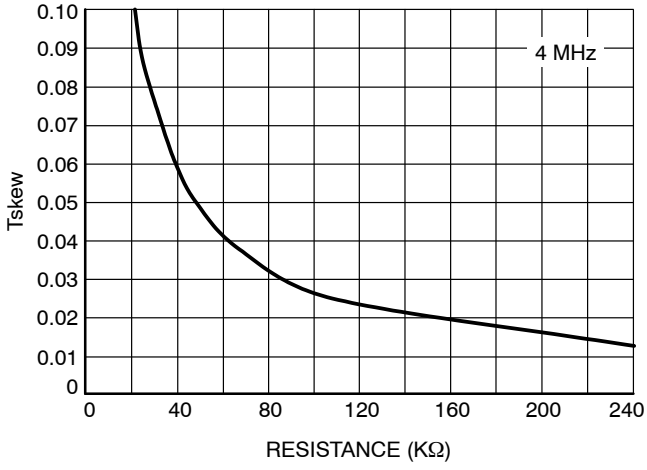


Figure 11. Tskew vs. Resistance (4 MHz, FS = 0)

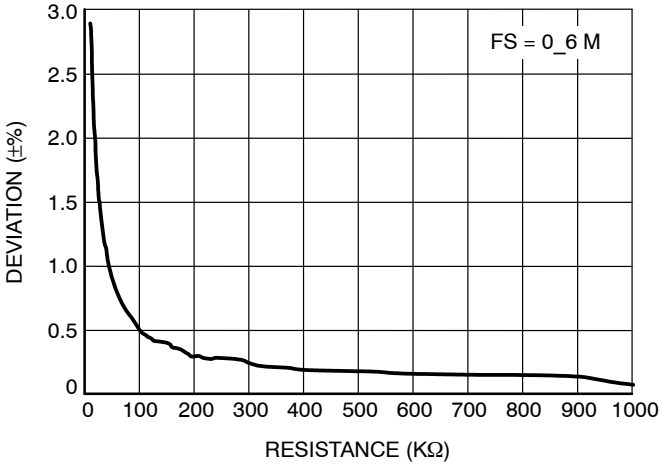


Figure 12. Deviation vs. Resistance (6 MHz, FS = 0)

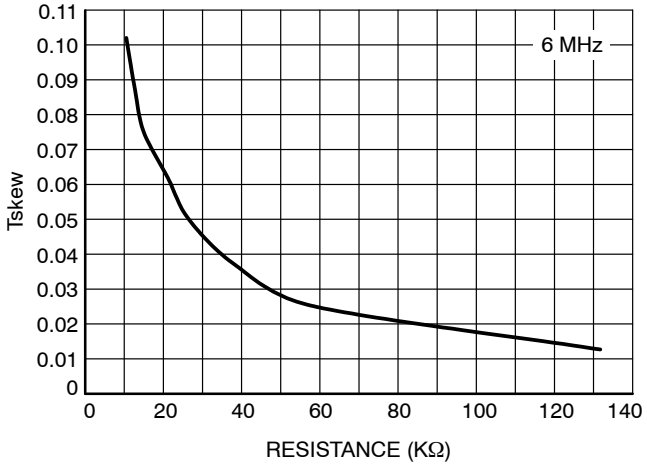


Figure 13. Tskew vs. Resistance (6 MHz, FS = 0)

TYPICAL CHARACTERISTICS (for V_{DD} = 2.5 V ± 0.2 V and 3.3 V ± 0.3 V)

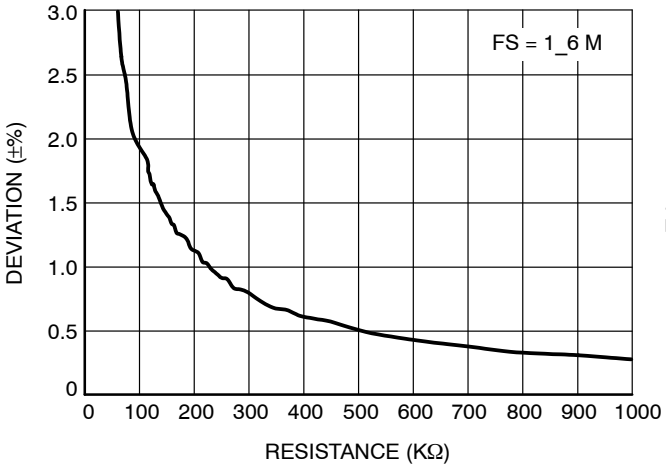


Figure 14. Deviation vs. Resistance (6 MHz, FS = 1)

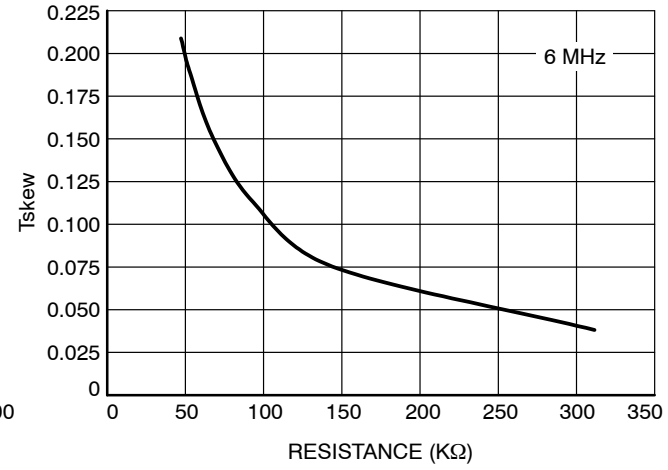


Figure 15. Tskew vs. Resistance (6 MHz, FS = 1)

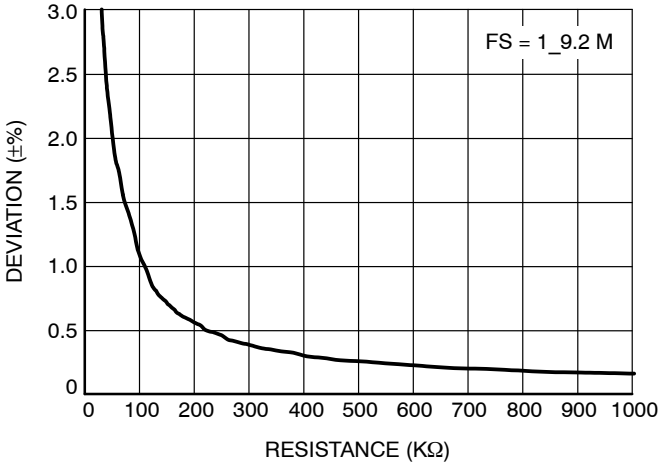


Figure 16. Deviation vs. Resistance (9.2 MHz, FS = 1)

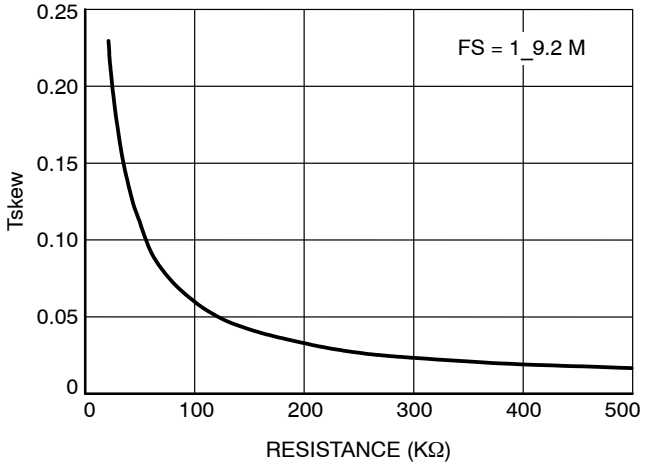


Figure 17. Tskew vs. Resistance (9.2 MHz, FS = 1)

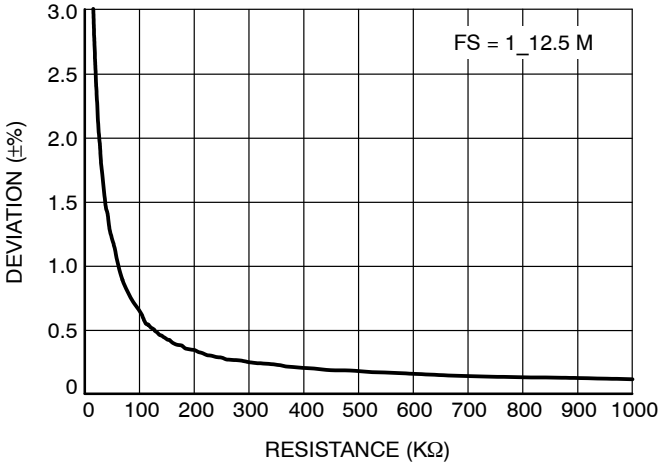


Figure 18. Deviation vs. Resistance (12.5 MHz, FS = 1)

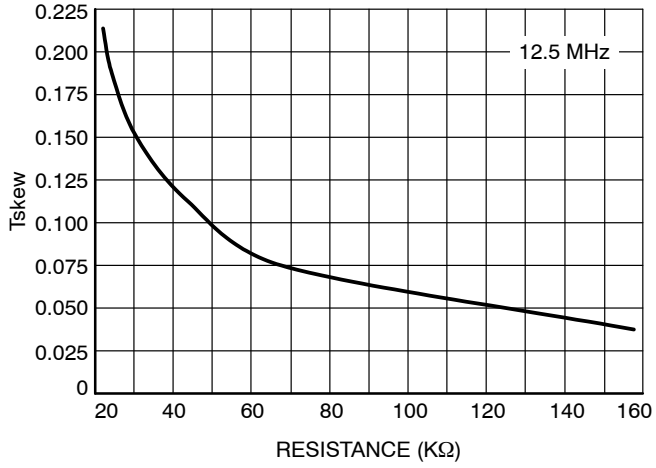


Figure 19. Tskew vs. Resistance (12.5 MHz, FS = 1)

TYPICAL CHARACTERISTICS (for V_{DD} = 2.5 V ± 0.2 V and 3.3 V ± 0.3 V)

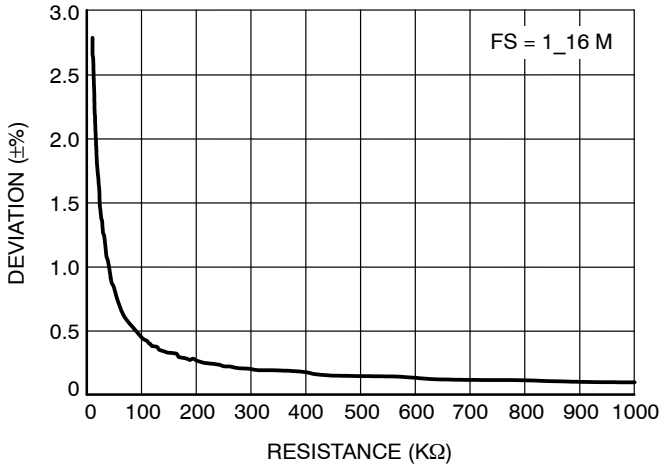


Figure 20. Deviation vs. Resistance (16 MHz, FS = 1)

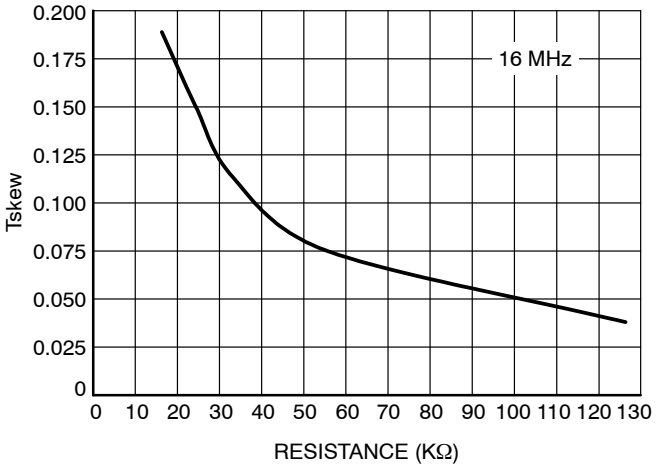


Figure 21. Tskew vs. Resistance (16 MHz, FS = 1)

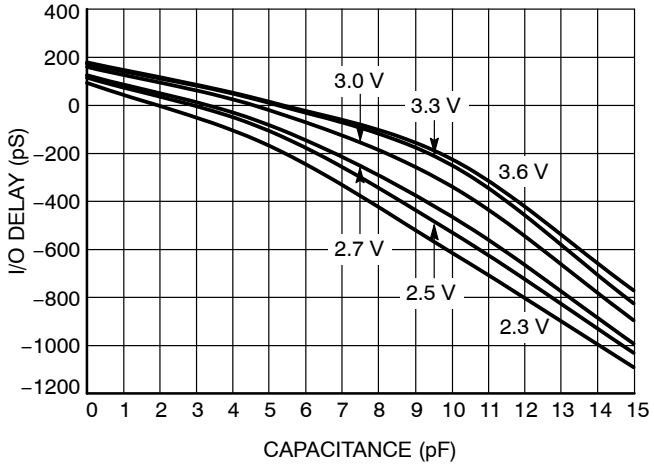


Figure 22. I/O Delay vs. Load (DLY_CTRL) (For 2 MHz, FS = 0)

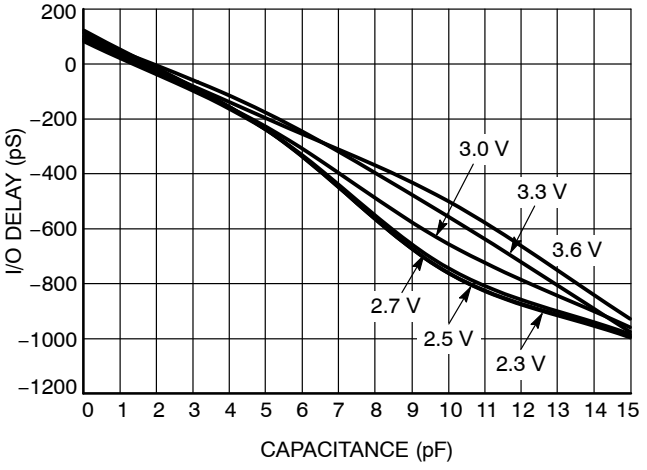


Figure 23. I/O Delay vs. Load (DLY_CTRL) (For 4 MHz, FS = 0)

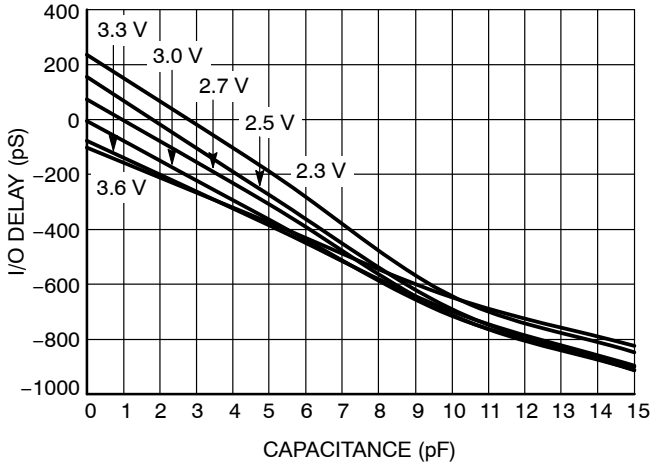


Figure 24. I/O Delay vs. Load (DLY_CTRL) (For 6 MHz, FS = 0)

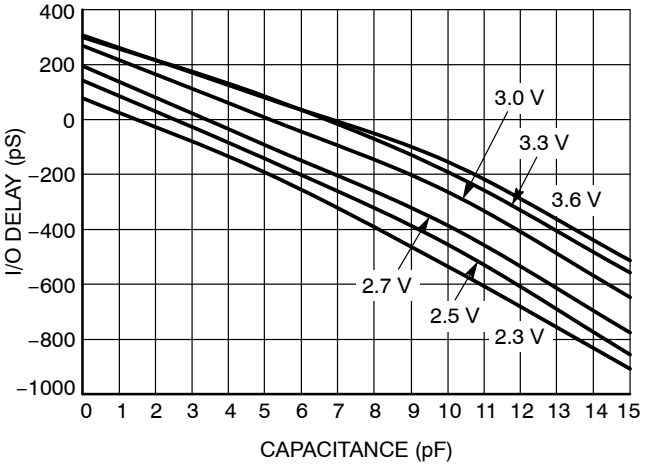


Figure 25. I/O Delay vs. Load (DLY_CTRL) (For 6 MHz, FS = 1)

TYPICAL CHARACTERISTICS (for V_{DD} = 2.5 V ± 0.2 V and 3.3 V ± 0.3 V)

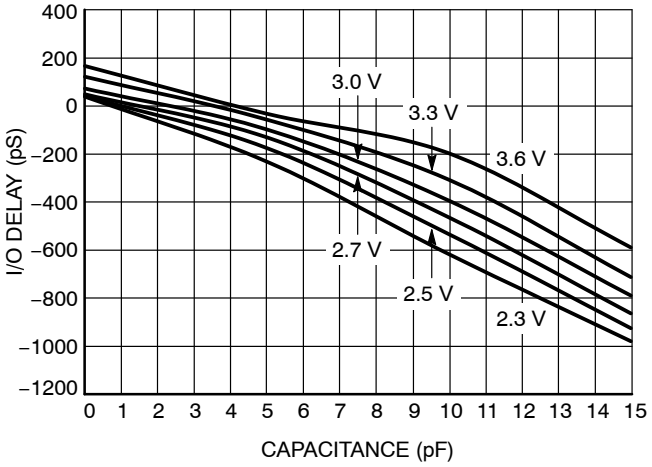


Figure 26. I/O Delay vs. Load (DLY_CTRL) (For 12.5 MHz, FS = 1)

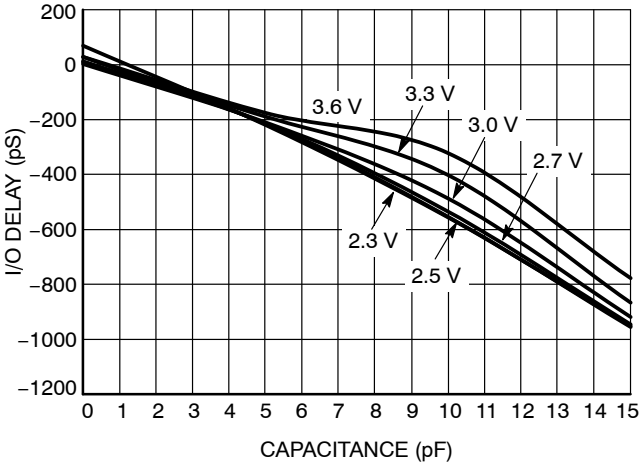
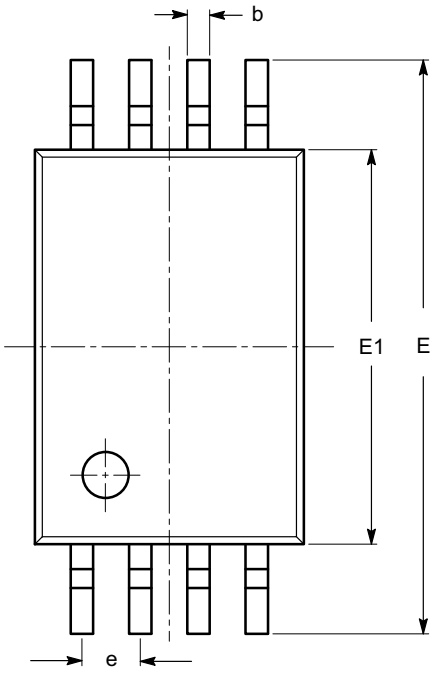


Figure 27. I/O Delay vs. Load (DLY_CTRL) (For 16 MHz, FS = 1)

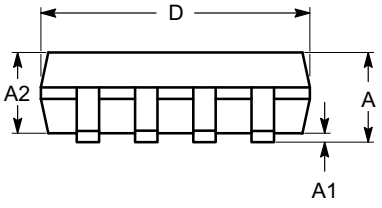
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

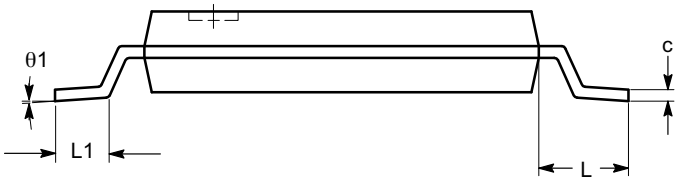


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



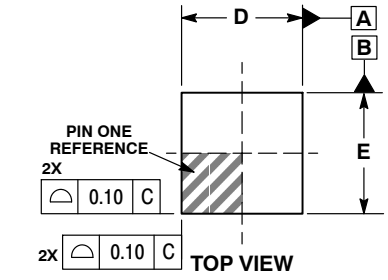
END VIEW

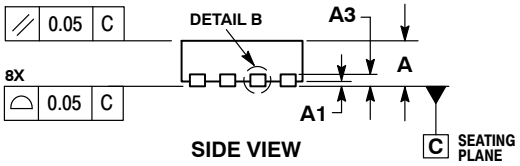
Notes:

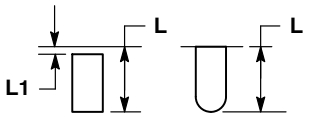
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

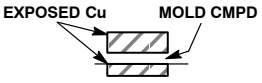
PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511AQ−01
ISSUE A



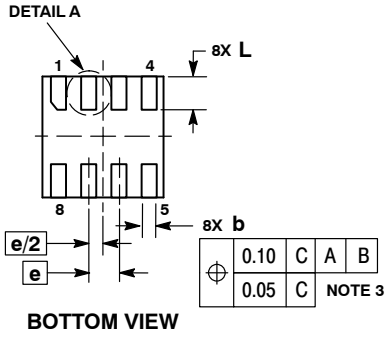




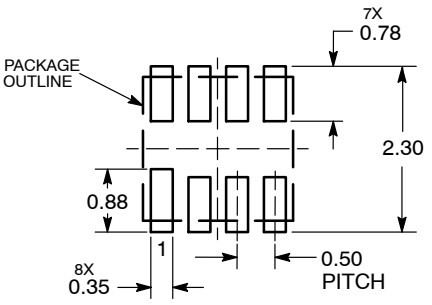


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 9. ORDERING INFORMATION

Ordering Code	Marking	Package Type	Temperature
PCS3P73Z01AWG−08−TT	3P73Z01AWG	8−pin 4.4−mm TSSOP − TUBE, Green	Commercial
PCS3P73Z01AWG−08−TR	3P73Z01AWG	8−pin 4.4−mm TSSOP − TAPE & REEL, Green	Commercial
PCS3P73Z01AWG−08−CR	AE1 LLYW	8−pin 2−mm TDFN COL − TAPE & REEL, Green	Commercial
PCS3I73Z01AWG−08−TT	3I73Z01AWG	8−pin 4.4−mm TSSOP − TUBE, Green	Industrial
PCS3I73Z01AWG−08−TR	3I73Z01AWG	8−pin 4.4−mm TSSOP − TAPE & REEL, Green	Industrial
PCS3I73Z01AWG−08−CR	AE2 LLYW	8−pin 2−mm TDFN COL − TAPE & REEL, Green	Industrial

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